WHAT IS CLAIMED IS:

1. A flip-flop circuit for reducing the current spike, comprising:

an input for receiving first data, said input being controlled by a first clock signal; and

an output for transmitting second data received by said input prior to said first data, said output being controlled by a second clock signal, said first and second clock signals having the same frequency and substantially the same phase, wherein the arrival times of said first and second clock signals at said flip-flop are at least slightly skewed.

2. The flip-flop of Claim 1, further comprising:

a first clock input for receiving said first clock signal; and

a second clock input for receiving said second clock signal.

3. The flip-flop of Claim 2, wherein said first clock input comprises two p-type field effect transistors connected together.

4. The flip-flop of Claim 3, wherein said second clock input comprises two n-type field effect transistors connected together.

5. The flip-flop of Claim 4, wherein a first one of said two p-type field effect transistors is connected in series with a first one of said two n-type field effect transistors.

6. The flip-flop of Claim 5, further comprising:

an additional n-type field effect transistor connected in series with said first p-type field effect transistor and said first n-type transistor, said additional n-type field effect transistor being controlled by said first clock signal.

7. A sequential logic circuit, comprising:

a first flip-flop having an input for receiving data and an output for transmitting said data, at least said output of said first flip-flop being controlled by a first clock signal;

combinational logic connected to said first flip-flop for receiving said data from said first flip-flop; and

a second flip-flop connected to said combinational logic having an input for receiving said data from said combinational logic and an output for transmitting said data, said input of said second flip-flop being controlled by said first clock signal, said output of said second flip-flop being controlled by a second clock signal, said first and second clock signals having the same frequency and substantially the same phase, wherein the arrival times of said first and second clock signals at said second flip-flop are at least slightly skewed.

8. The logic circuit of Claim 7, wherein said second flip-flop further comprises:

a first clock input for receiving said first clock signal; and

a second clock input for receiving said second clock signal.

9. The logic circuit of Claim 8, wherein said first clock input comprises two p-type field effect transistors connected together, and said second clock input comprises two n-type field effect transistors connected together.

10. The logic circuit of Claim 9, wherein a first one of said two p-type field effect transistors is connected in series with a first one of said two n-type field effect transistors.

11. The logic circuit of Claim 10, wherein said second flip-flop further comprises:

an additional n-type field effect transistor connected in series with said first p-type field effect transistor and said first n-type transistor, said additional n-type field effect transistor being controlled by said first clock signal.

12. A method for reducing current spikes within a logic circuit, comprising the steps of:

receiving data by a first flip-flop;

transmitting said data to combinational logic connected to said first flip-flop, said step of transmitting being controlled by a first clock signal;

receiving said data on an input of a second flip-flop connected to said combinational logic, said step of receiving being controlled by said first clock signal; and

transmitting said data through an output of said second flip-flop, said step of transmitting being controlled by a second clock signal, said first and second clock signals having the same frequency and substantially the same phase, wherein the arrival times of said first and second clock signals at said second flip-flop are at least slightly skewed.

13. The method of Claim 12, further comprising the steps of:

receiving at a first clock input of said second flip-flop said first clock signal; and

receiving at a second clock input of said second flip-flop said second clock signal.

14. The method of Claim 13, further comprising the step of:

reducing short-circuit current in said second flip-flop using an n-type field effect transistor connected in series with said first and second clock inputs, said n-type field effect transistor being controlled by said first clock signal.